R16

Reg. No:

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech II Year II Semester Supplementary Examinations Dec 2019
PULSE AND DIGITAL CIRCUITS
(Electronics & Communication Engineering)

Time: 3 hours   Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1 a Explain the operation of RC Differentiator circuit and sketch the response for step input.   **7M**

   b If a Pulse of 5V amplitude and pulse width of 0.5msec is applied to High Pass RC circuit consisting of R=22KΩ and C=0.47 µF, Calculate % Tilt of the output waveform.   **5M**

OR

2 a Explain the response of RC low pass circuit for exponential input signal   **6M**

   b A symmetrical square wave of amplitude ±5v and frequency of 2 KHz is impressed on an RC low pass circuit. If R= 5KΩ, C=0.1µf, Calculate and plot the steady state output with respect to time.   **6M**

UNIT-II

3 a Draw the basic circuit diagram of positive peak clamper circuit and explain its operation.   **6M**

   b Explain the effect of diode characteristics on clamping voltage.   **6M**

OR

4 a Draw the diode comparator circuit and explain the operation when ramp input signal is applied.   **6M**

   b Write short notes on   **6M**
      I. Diode switching times
      II. Synchronized clamping.

UNIT-III

5 a Design a free running multivibrator to generate a square wave of amplitude 10 V and frequency of 1 KHz with 70% duty cycle.   **7M**

   b Apply appropriate triggering technique to a collector coupled bistable multivibrator and explain briefly.   **5M**

OR

6 a With the help of neat circuit diagram, Explain the working of Collector- Coupled one-shot multivibrator.   **7M**

   b Design a Collector-Coupled one-shot multivibrator with the following specifications. Output pulse duration=500 m sec , h$_{FE(min)}$= 25, Ic(sat) = 5 mA, V$_{CC}$= 10 V, V$_{BB}$= - 4 V, V$_{CE(sat)}$= 0.4 V, V$_{BE(sat)}$ = 0.8 V.   **5M**

UNIT-IV

7 a In a current sweep circuit, explain how linearity correction is made through adjustment of driving waveform.   **7M**

   b Write the basic mechanism of transistor television sweep circuit.   **5M**

OR

8   a   Explain the basic principles of the miller and bootstrap time base generators.   **6M**

    b   With the help of neat circuit diagram and waveforms, explain the working of a   **6M**
transistor constant current sweep circuit.

UNIT-V

9   a   What is sampling gate? Explain how it differs from Logic gates.   **4M**

    b   What is pedestal? How it affects the output of a sampling gates.   **5M**

    c   What are the drawbacks of two diode sampling gate?   **3M**

OR

10   a   With the help of neat circuit diagrams and truth table explain the working of a DTL   **6M**
and RTL NAND gate.

    b   Compare the different logic families in terms of propagation delay, power   **6M**
dissipation, Noise margin, fan-in and fan-out.

*** END ***